

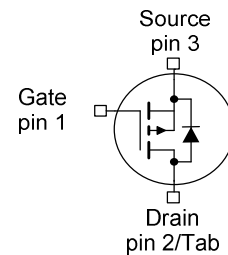
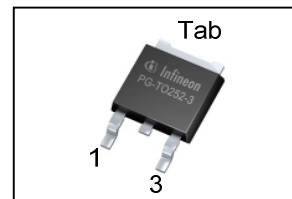
**OptiMOS®-P2 Power-Transistor**

**Features**

- P-channel - Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

**Product Summary**

$V_{DS}$	-40	V
$R_{DS(on)}$	4.3	mΩ
$I_D$	-90	A

**PG-TO252-3-313**


Type	Package	Marking
IPD90P04P4L-04	PG-TO252-3-313	4P04L04

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=-10\text{V}$	-90	A
		$T_C=100\text{ °C}$ , $V_{GS}=-10\text{V}^{2)}$	-90	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	-360	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=-45\text{A}$	60	mJ
Avalanche current, single pulse	$I_{AS}$	-	-90	A
Gate source voltage	$V_{GS}$	-	$\pm 16^{3)}$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	125	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>2)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$	-	-	-	1.2	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>4)</sup>	-	-	40	

**Electrical characteristics**, at  $T_j=25\text{ °C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-1mA$	-40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.7	-2.2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=-32V, V_{GS}=0V, T_j=25\text{ °C}$	-	-0.08	-1	$\mu A$
		$V_{DS}=-32V, V_{GS}=0V, T_j=125\text{ °C}^{2)}$	-	-20	-200	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=-16V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-85A$	-	5.1	6.6	m $\Omega$
		$V_{GS}=-10V, I_D=-90A$	-	3.6	4.3	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	8900	11570	pF
Output capacitance	$C_{oss}$		-	2532	3800	
Reverse transfer capacitance	$C_{rss}$		-	100	200	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-90A,$ $R_G=3.5\Omega$	-	20	-	ns
Rise time	$t_r$		-	20	-	
Turn-off delay time	$t_{d(off)}$		-	140	-	
Fall time	$t_f$		-	60	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=-32V, I_D=-90A,$ $V_{GS}=0$ to $-10V$	-	31	40	nC
Gate to drain charge	$Q_{gd}$		-	24	48	
Gate charge total	$Q_g$		-	135	176	
Gate plateau voltage	$V_{plateau}$		-	-3.5	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25^\circ C$	-	-	-90	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	-360	
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_F=-90A,$ $T_j=25^\circ C$	-	-1	-1.3	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=-20V, I_F=-50A,$ $di_F/dt=-100A/\mu s$	-	63	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	72.3	-	nC

<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC} = 1.2K/W$  the chip is able to carry -136A at 25°C.

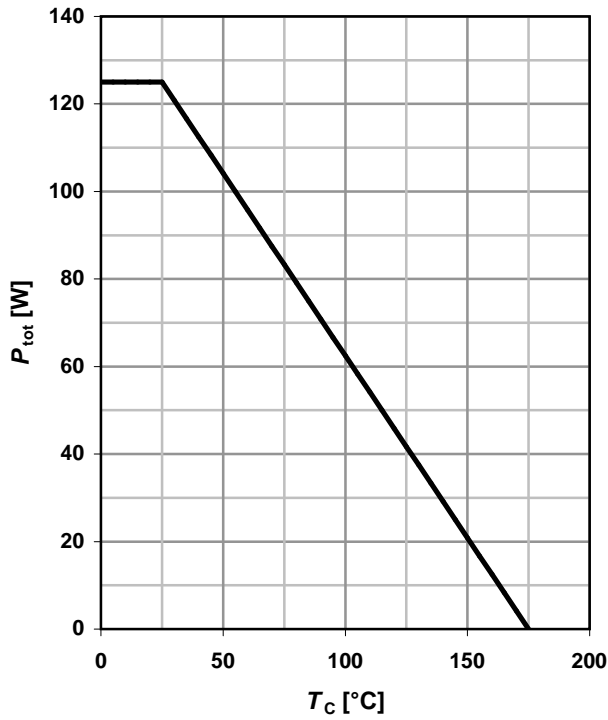
<sup>2)</sup> Defined by design. Not subject to production test.

<sup>3)</sup>  $V_{GS}=+5V/-16V$  according AEC;  $V_{GS}=+16V$  for max 168h at  $T_j=175^\circ C$

<sup>4)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

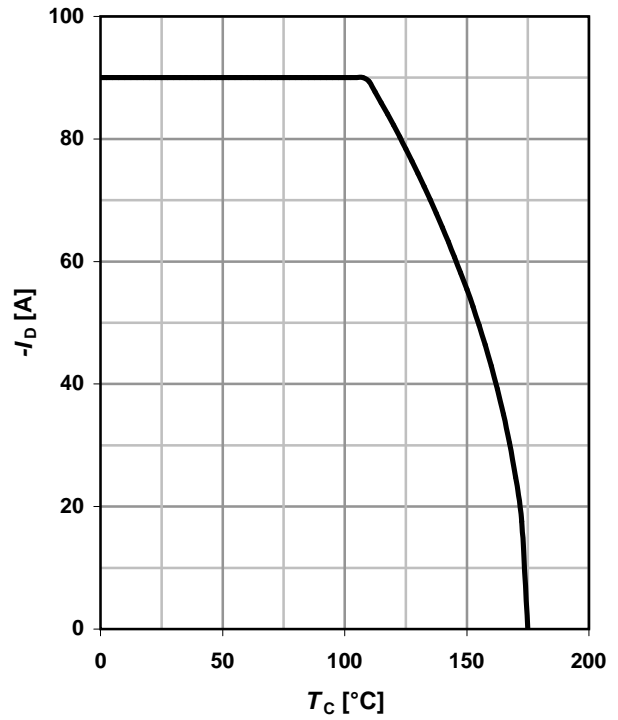
**1 Power dissipation**

$P_{tot} = f(T_C); V_{GS} \leq -6V$



**2 Drain current**

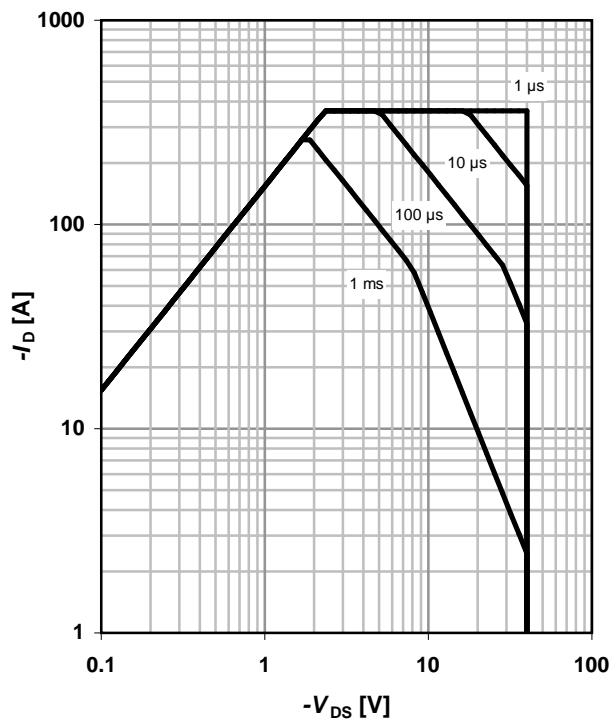
$I_D = f(T_C); V_{GS} = -10V$



**3 Safe operating area**

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

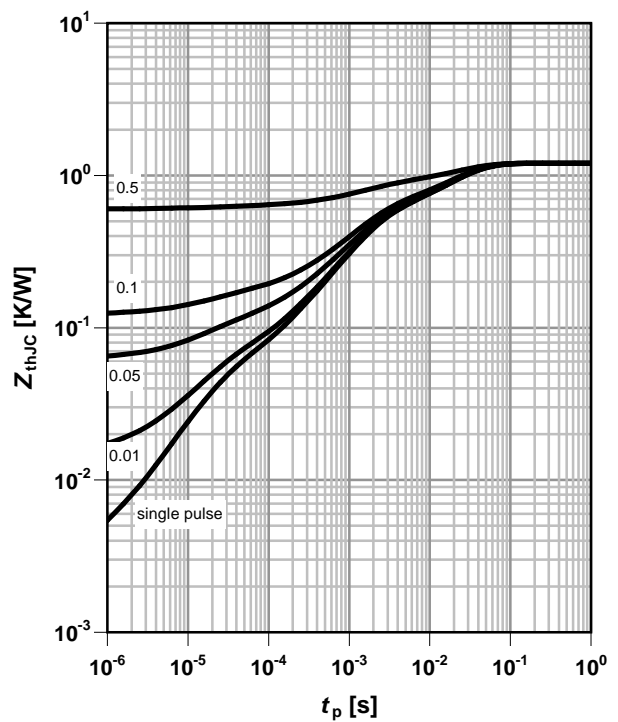
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC} = f(t_p)$

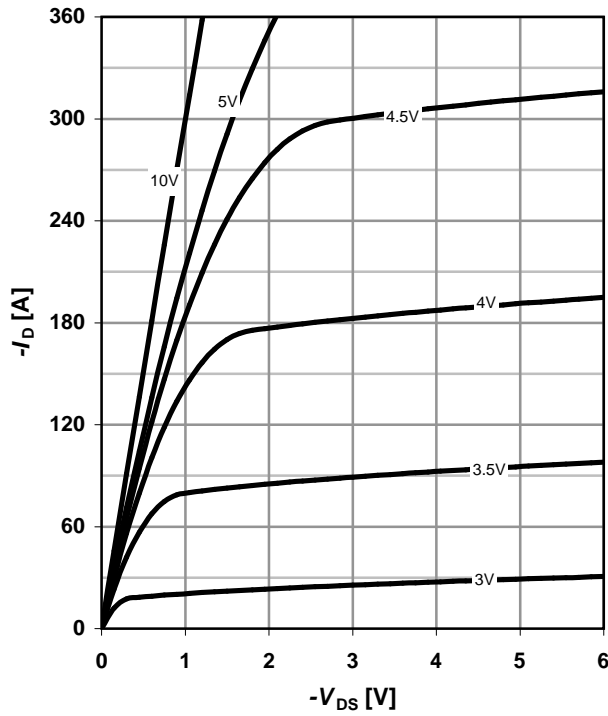
parameter:  $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

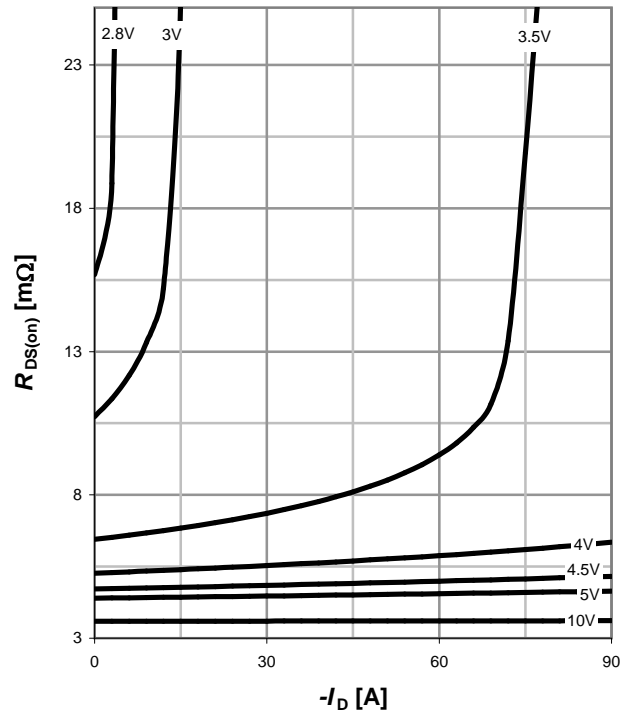
parameter:  $-V_{GS}$



**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

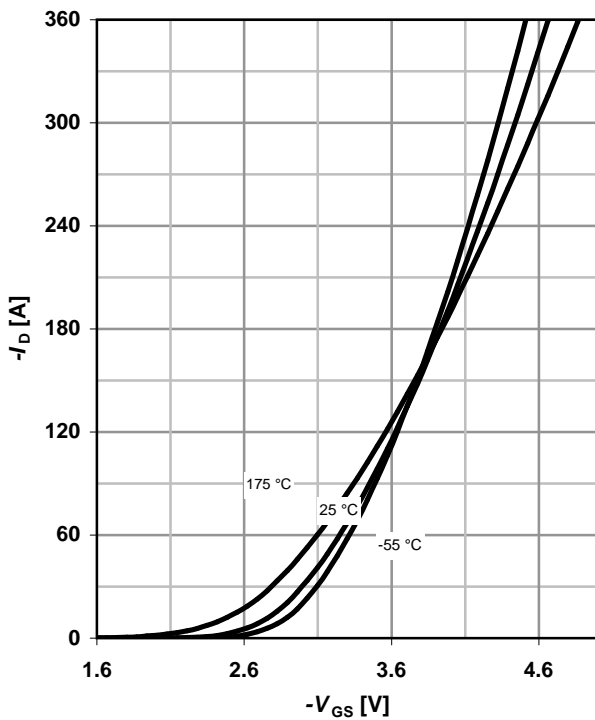
parameter:  $-V_{GS}$



**7 Typ. transfer characteristics**

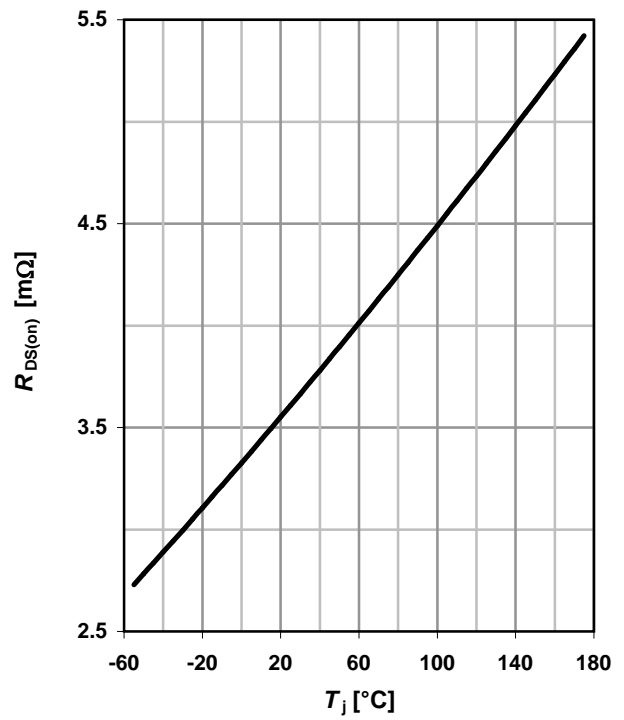
$I_D = f(V_{GS}); V_{DS} = -6V$

parameter:  $T_j$



**8 Typ. drain-source on-state resistance**

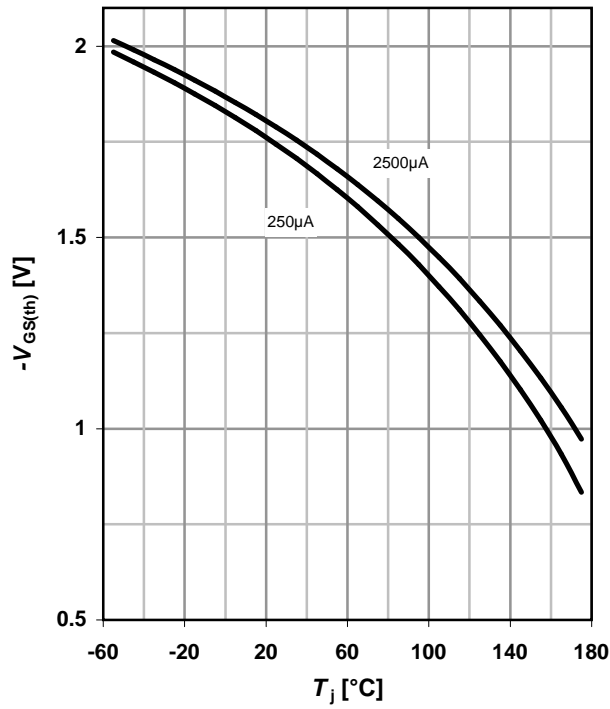
$R_{DS(on)} = f(T_j); I_D = -70\text{ A}; V_{GS} = -10\text{ V}$



**9 Typ. gate threshold voltage**

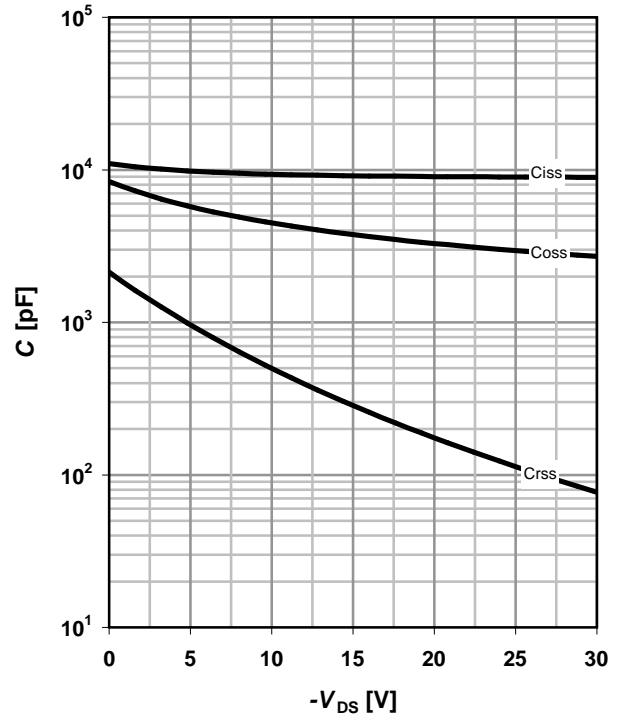
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $-I_D$



**10 Typ. capacitances**

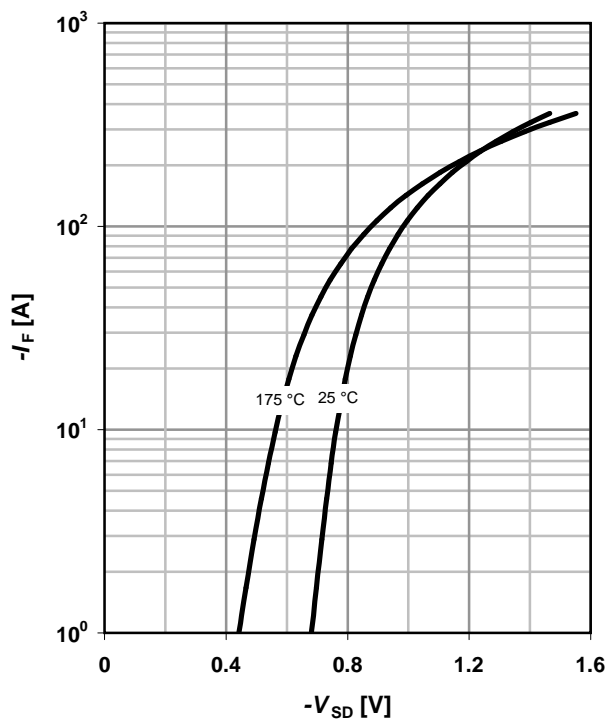
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



**11 Typical forward diode characteristics**

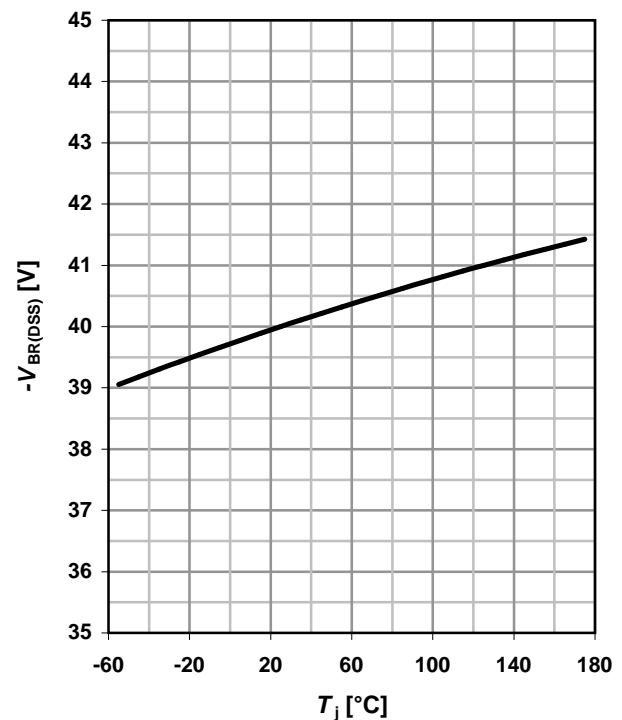
$I_F = f(V_{SD})$

parameter:  $T_j$



**12 Drain-source breakdown voltage**

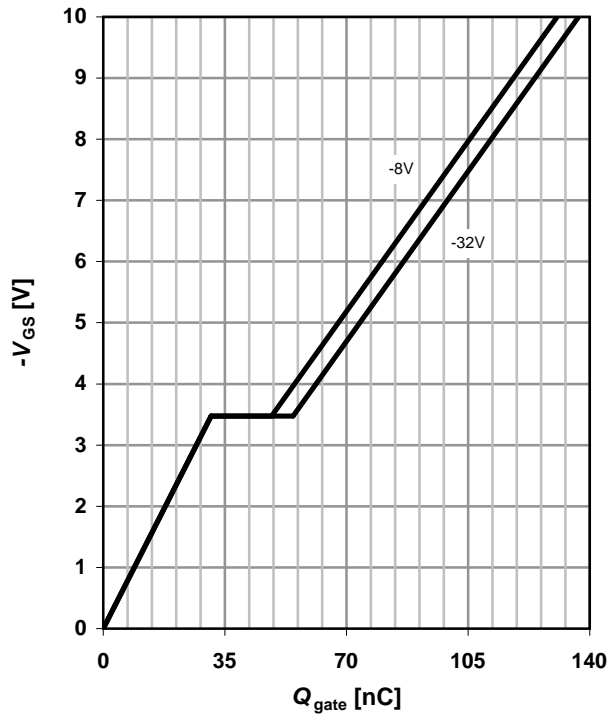
$V_{BR(DSS)} = f(T_j); I_D = -1 mA$



**13 Typ. gate charge**

$V_{GS} = f(Q_{gate}); I_D = -90 \text{ A pulsed}$

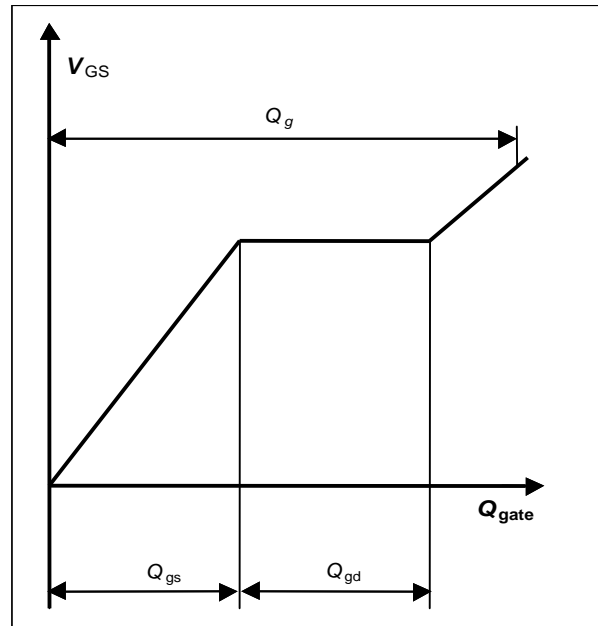
parameter:  $V_{DD}$



**14 Gate charge waveforms**

$V_{GS} = f(Q_{gate}); I_D = -90 \text{ A pulsed}$

parameter:  $V_{DD}$



**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

**© Infineon Technologies AG 2011**  
**All Rights Reserved.**

#### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

#### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### **Warnings**

Due to technical requirements, components may contain dangerous substances.  
For information on the types in question, please contact the nearest Infineon Technologies Office.  
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life.  
If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.



## Revision History

Version	Date	Changes
0.1	29.01.2010	Initial Target Data Sheet
0.2	16.12.2010	Preliminary Data Sheet
1.0	27.04.2011	Final Data Sheet